L1 ANSWER 1 OF 1 CAPLUS COPYRIGHT 2004 ACS on STN
AN 2002:446195 CAPLUS
DN 137:26833
TI Trench-capacitor vertical transistor DRAM cell
IN Yamada, Takashi; Kajiyama, Takeshi
PA Kabushiki Kaisha Toshiba, Japan
IC ICM H01L021-8242
ICS H01L029-786; H01L027-108
CC 76-3 (Electric Phenomena)

PI	EP 1213761	A1	20020612	EP 2001-127355 20011121
	JP 2002176154	A2	20020621	JP 2000-371106 20001206
	US 2002076880	A1	20020620	US 2001-993967 20011127
	CN 1357924	A	20020710	CN 2001-142970 20011206
				JP 2000-371106 A 20001206

AB A method is claimed for fabrication of a DRAM cell without variation of the transistor characteristics. A semiconductor device has an element substrate including a semiconductor layer of a 1st conductivity type being formed over a semiconductor substrate with a dielec. film interposed there between. A groove is formed in the element substrate with a depth extending from a top surface of the semiconductor layer into the dielec. film, the groove having a width-increased groove portion in the dielec. film as to expose a bottom surface of the semiconductor layer. An impurity diffusion source is buried in the width-increased groove portion to be contacted with the bottom surface. A transistor is formed to have a 1st diffusion layer being formed through impurity diffusion from the impurity diffusion source to the bottom surface of the semiconductor layer, a 2nd diffusion layer formed through impurity diffusion to the top surface of the semiconductor layer, and a gate electrode formed at a side face of the groove over the impurity diffusion source with a gate insulation film between the side face and the gate electrode.

ST capacitor transistor DRAM fabrication
IT Memory devices
(DRAM (dynamic random access); trench-capacitor vertical transistor DRAM cell)
IT Capacitors
Diffusion
Doping
Semiconductor memory devices
Transistors
(trench-capacitor vertical transistor DRAM cell)
RE.CNT 8 THERE ARE 8 CITED REFERENCES AVAILABLE FOR THIS RECORD

PAT-NO: JP401147860A
DOCUMENT-IDENTIFIER: JP 01147860 A
TITLE: SEMICONDUCTOR MEMORY AND MANUFACTURE THEREOF
PUBN-DATE: June 9, 1989

INVENTOR-INFORMATION:
NAME
EMA, TAIJI

ASSIGNEE-INFORMATION:
NAME COUNTRY
FUJITSU LTD N/A

APPL-NO: JP62306414
APPL-DATE: December 3, 1987

INT-CL (IPC): H01L027/10, H01L027/04
US-CL-CURRENT: 257/E27.096, 365/174 , 438/396 , 438/FOR.212

ABSTRACT:
PURPOSE: To improve breakdown strength by providing thick insulating films between the elements of semiconductor layers for forming the active regions of
transfer transistors, and between the semiconductor and an opposite electrode.
CONSTITUTION: Thick insulating films are provided between elements of semiconductor layers 13 for forming the active regions of transfer transistors
T<SB>1</SB>, and between the layer 13 and an opposite electrode 11a. Thus, the
impurity concentration of a semiconductor substrate 11 for forming the electrode 11a is enhanced, or the electrode 11a is formed on a conductive film.
Further, after a first insulating film 12 and a second insulating film 14 having the semiconductor layer are formed on the substrate 11 which becomes the
electrode 11a, a groove 17 is formed. Thus, the active region of the transistor T<SB>1</SB> is formed on the sidewall of the groove 17 interposed with the films 12, 14, a storage electrode 19a can be formed in the groove 17,
thereby improving breakdown strength.

X in EP SR

このようにして、対向電極１１ａとなるSi基板１１上にSiO₂膜１２とSi層１３を有するSiO₂膜１４とを形成し、さらに不純物を含有するポリSi膜１５によりビット線ＢＬ₁を形成し、その後に溝部１７を形成している。このため転送トランジスタの能動領域はSiO₂膜１２、１４を介在した溝部１７の側壁に形成し、蓄積電極１９ａを溝部１７内に形成することができる。

これにより、各転送トランジスタＴ₁の能動領域間及び該能動領域と対向電極１１ａとの間の絶縁耐力を向上させることが可能となる。

〔発明の効果〕

以上説明したように本発明によれば転送トランジスタ間の絶縁や該転送トランジスタと蓄積容量との間の絶縁耐力を向上させることができる。このため、パンチスルーや空之層容量の介入に伴う従来の問題を解決することが可能となる。

これにより超微細、高集積度及び高性能の半導体記憶装置を製造することが可能となる。

4．図面の簡単な説明

第１図は本発明の実施例に係るＤＲＡＭセルの構造図、

第２図は本発明の実施例に係るＤＲＡＭセルの形成工程図、

第３図は従来例に係るＤＲＡＭセルの説明図である。

（符号の説明）

Ｔ，Ｔ₁…転送トランジスタ、

Ｃ，Ｃ₁…蓄積容量、

１，１１…Si基板（半導体基板）、

１ｂ，１１ａ…対向電極、

１ａ…Ｐ⁺Si膜、

１ｂ…Ｐ⁺⁺Si膜、

２…フィールド酸化膜、

１２、１４…SiO₂膜（第１、２の絶縁膜又は絶縁層）、

３…ドレイン、

１３…Si層（半導体層）、

４…ソース（ビット線ＢＬ₁）、

５，７…SiO₂膜、

２２…SiO₂膜（第４の絶縁膜）、

１５…ポリSi膜（第１の導電体層又はビット線）、

６，１９ａ…蓄積電極（ポリSi膜）、

１８…SiO₂膜又はSi₃N₄膜（第３の絶縁膜）、

１８ａ…誘電体膜、

８，１７…溝部、

９…空之層、

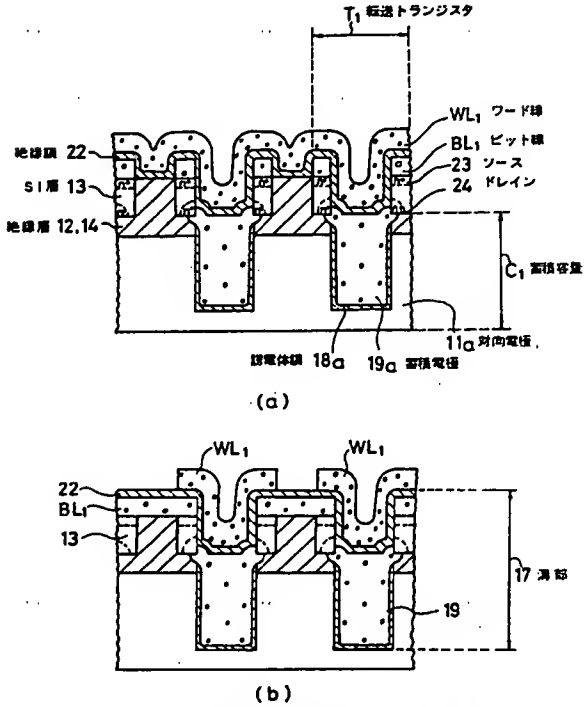
１６，２０…開口部、

１９，２１，２５…ポリSi膜（第２，３，４の導電体層）、

ＷＬ，ＷＬ₁…ワード線、

ＢＬ，ＢＬ₁…ビット線、

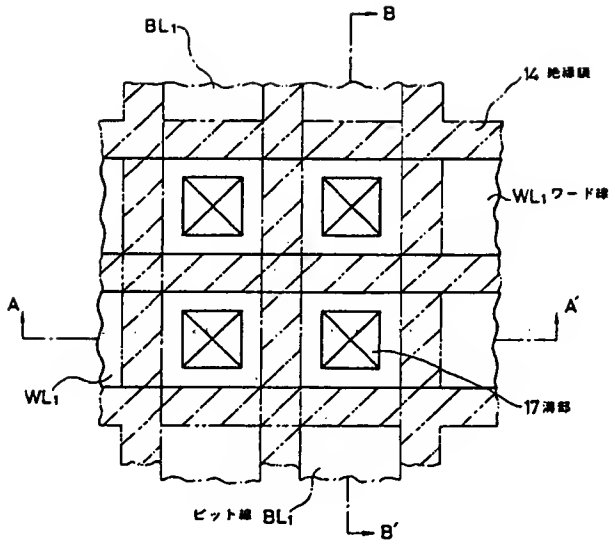
ｄ…深さ。



本発明の実施例に係るDRAMセルの構造図

第 1 図（その１）

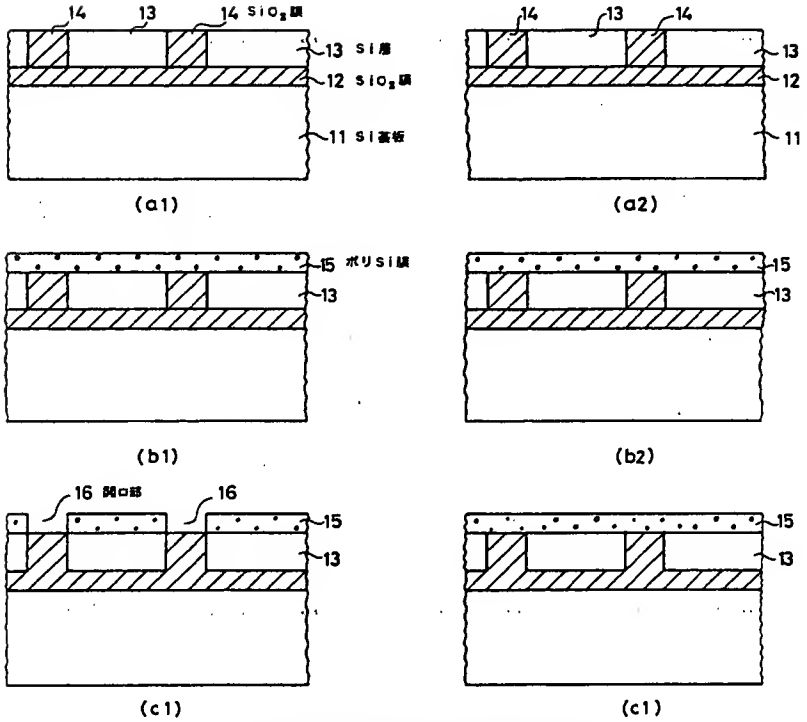
代理人弁理士　井桁　貞一



(c)

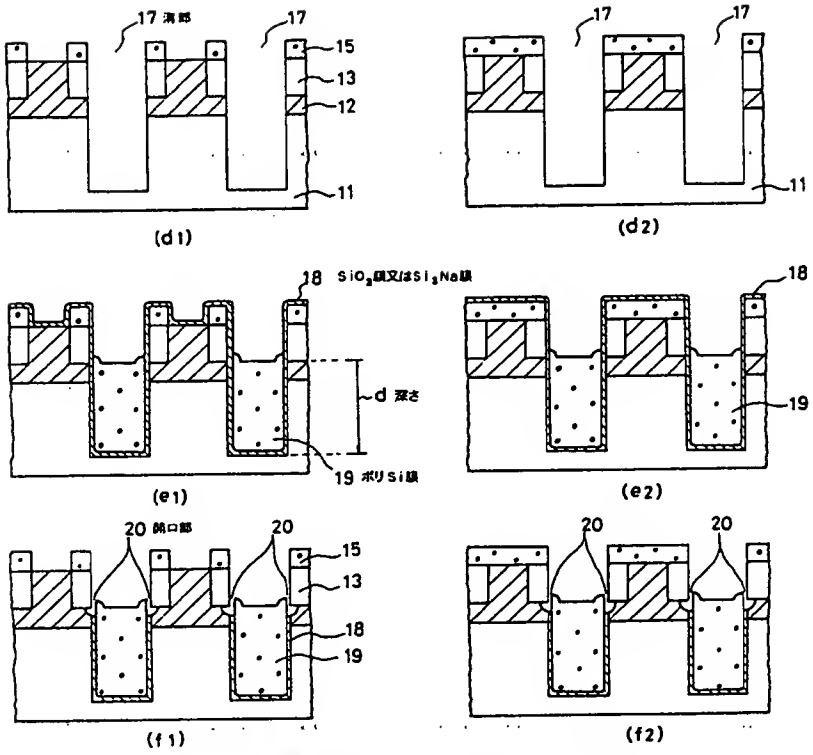
本発明の実施例に係るDRAMセルの構造図

第 1 図（その2）



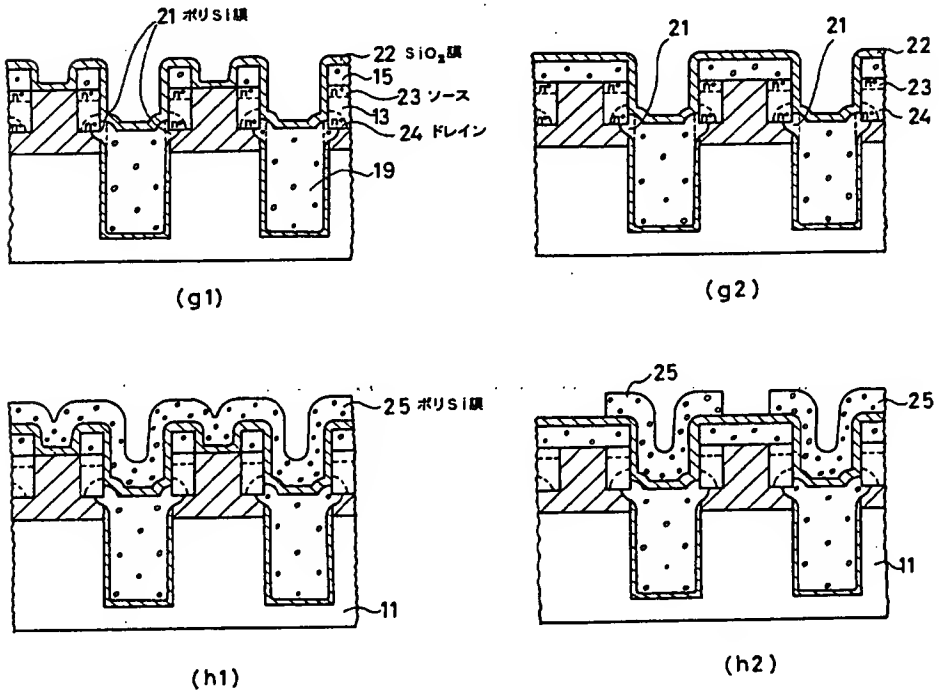
本発明の実施例に係るDRAMセルの形成工程図

第 2 図（その1）



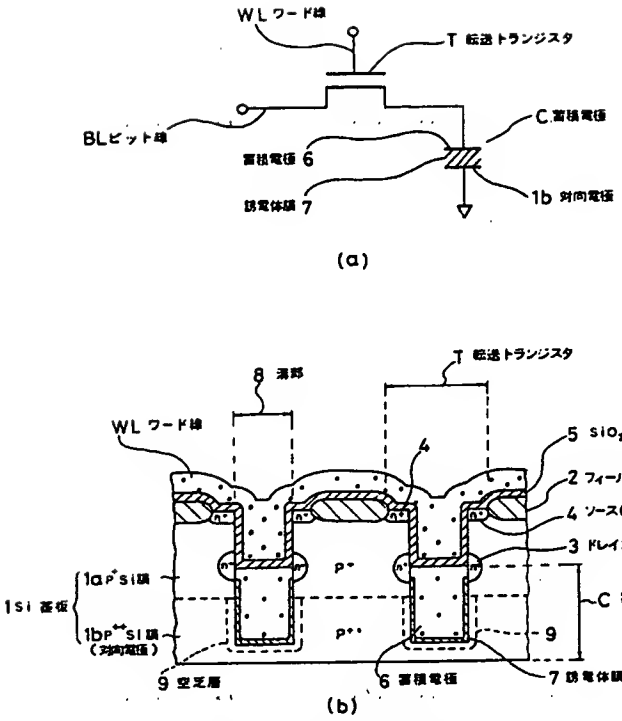
本発明の実施例に係るDRAMセルの形成工程図

第 2 図（その2）



本発明の実施例に係るDRAMセルの形成工程図

第 2 図（その3）



従来例に係るDRAMセルの構造図

第 3 図

PAT-NO: JP401158768A
DOCUMENT-IDENTIFIER: JP 01158768 A

TITLE: SEMICONDUCTOR STORAGE DEVICE AND ITS MANUFACTURE

PUBN-DATE: June 21, 1989

INVENTOR-INFORMATION:
NAME
EMA, YASUMI
ASSIGNEE-INFORMATION:
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FUJITSU LTD N/A

APPL-NO: JP62318011
APPL-DATE: December 15, 1987
INT-CL (IPC): H01L027/10
US-CL-CURRENT: 257/302, 257/304 , 257/305 , 257/E27.096 , 438/396

ABSTRACT:

PURPOSE: To facilitate avoidance of generating a depletion layer capacitance
by providing thick 1st insulating films between 2nd semiconductor layers which
constitute active regions of respective transfer transistors and a 1st semiconductor layer which is to be a facing electrode.

CONSTITUTION: A facing electrode 11a is comprises an n-type or p-type Si substrate 11 and constitutes a storage capacitance C<SB>1</SB>. Insulating films 12 provide element isolation between active regions of transfer transistors T<SB>1</SB> and the facing electrode 11a and are made of SiO<SB>2</SB> films or the like. By providing the insulating films, a conductive film such as a P<SP>++</SP> type Si substrate or a metal film can be
used as the facing electrode 11a. The active regions of the transfer transistors T<SB>1</SB> comprises Si substrates 13. Thus, the thick SiO<SB>2</SB> films 12 are provided between the Si substrates 13 constituting the active regions of the transfer transistors T<SB>1</SB> and the facing electrode 11a. Therefore, the impurity concentration of the Si substrate 11 can be increased by a conductive film can be used as the facing electrode 11a.
With this constitution, generation of a depletion layer capacitance can be avoided.

X in SP SR